WHAT IS CLAIMED IS:

1. In a wire-bond package arrangement including a substrate; at least one semiconductor chip mounted on said substrate; and at least one each of a power ring, a ground ring and a signal ring at the height of the substrate surfaces mounting said at least one chip being operatively connected to circuitry on said chip by wires; the improvement comprising:

a) said at least one power ring and ground ring being located in an interstitial pattern on the surface of said substrate;

b) a first wire extending within a vertical height between the surface of the substrate and the surface of said chip said wire commonly interconnecting said interstitial pattern formed by said at least one power and ground ring with circuitry on said chip; and

c) a second wire extending in a vertical loop spaced above said first vertical wire loop and interconnecting circuitry on said chip with said at least one signal ring.

2. A wire-bond package arrangement as claimed in Claim 1, wherein said chip, and said first and second wires on said substrate are encapsulated with an encapsulant so as to form a low-profile wire-bond package arrangement of specified overall height.

3. A wire-bond package arrangement as claimed in Claim 1, wherein said at least one power ring comprises a voltage bus and said at least one ground ring comprises a ground bus, wherein the interstitial pattern of said buses enables the provision of a single row of wire-bond connections on the substrate to simulate a single ring.

4. A wire-bond package arrangement as claimed in Claim 2, wherein said arrangement comprises a chip-up package having a reduced height wire loop to facilitate forming of an increased thickness of an encapsulant over said chip wires while maintaining the overall height of said package arrangement within specified parameters.

5. A wire-bond package arrangement as claimed in Claim 2, wherein said arrangement comprises a cavity-down plastic ball grid array package having a reduced height of wire loop to facilitate forming of an increased thickness of encapsulant over said chip and wires while maintaining the overall height of said package within specified parameters.

6. A wire-bond package arrangement as claimed in Claim 3; wherein there is provided a second voltage bus; and a second signal wire-bond ring with interstitial power connections facilitating the connection thereof with circuitry on said chip through a second wire loop formed by a third wire extending in elevation spaced above said second wire forming said first wire loop.

7. A wire-bond package arrangement as claimed in Claim 6, wherein said chip, said first wire and said first and second wire loops formed by said second and third wire-bond wires are encapsulated with an encapsulant so as to form a low-profile wire-bond package of specified overall height.

8. In a method of forming a wire-bond package arrangement including a substrate; at least one semiconductor chip mounted on said substrate; and at least one each of a power ring, a ground ring and a signal ring at the height of the substrate surfaces mounting said at least one chip being operatively connected to circuitry on said chip by wires; the improvement comprising:

a) locating said at least one power ring and ground ring being located in an interstitial pattern on the surface of said substrate;

b) having a first wire extending in a vertical height between the surface of the substrate and the surface of said chip said wire commonly interconnecting said interstitial pattern formed by said at least one power and ground ring with circuitry on said chip; and

c) extending a second wire in a vertical loop spaced above said first vertical wire loop and interconnecting circuitry on said chip with said at least one signal ring.

9. A method of forming a wire-bond package arrangement as claimed in Claim 8, wherein said chip, and said first and second wires on said substrate are encapsulated with an encapsulant so as to form a low-profile wire-bond package arrangement of specified overall height.

10. A method of forming a wire-bond package arrangement as claimed in Claim 8, wherein said at least one power ring comprises a voltage bus and said at least one ground ring comprises a ground bus, wherein the interstitial pattern of said buses enables the provision of a single row of wire-bond connections on the substrate to simulate a single ring.

11. A method of forming a wire-bond package arrangement as claimed in Claim 9, wherein said arrangement comprises a chip-up package having a reduced height wire loop to facilitate forming of an increased thickness of an encapsulant over said chip wires while maintaining the overall height of said package arrangement within specified parameters.

12. A method of forming wire-bond package arrangement as claimed in Claim 9, wherein said arrangement comprises a cavity-down plastic ball grid array package having a reduced height of wire loop to facilitate forming of an increased thickness of encapsulant over said chip and wires while maintaining the overall height of said package within specified parameters.

13. A method of forming a wire-bond package arrangement as claimed in Claim 10, wherein there is provided a second voltage bus; and a second signal wire-bond ring with interstitial power connections facilitating the connection thereof with circuitry on said chip through a second wire loop formed by a third wire extending in elevation spaced above said second wire forming said first wire loop.

14. A method of forming a wire-bond package arrangement as claimed in Claim 6, wherein said chip, said first wire and said first and second wire loops formed by said second and third wire-bond wires are encapsulated with an encapsulant so as to form a low-profile wire-bond package of specified overall height.